1. (Previously amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein said horizontally etched layer is a polysilicon layer and is etched a distance greater than a thickness of said polysilicon layer;

providing a wet etching to remove a final one of said multiple layers;

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

2. (Original) The method as described in claim 1 wherein the step of providing a horizontal etching determines that the dimensions of the base region are wider than the dimensions of the doped collector region and the emitter region.

3. (Original) The method as described in claim 1 further comprising the step of providing a surface oxide layer and polysilicon layer as 2 of the multiple layers.

4. (Original) The method as described in claim 3 further comprising the step of providing an oxide layer and a Nitride layer above said layers of surface oxide and polysilicon.

5. (Original) The method as described in claim 1 further comprising the step of doping the collector region with phosphorus or arsenic, using ion implantation.

6. (Withdrawn)

7. (Original) The method as described in claim 1 further comprising the step of using an isotropic plasma etch to perform said wet etching.

8. (Currently amended) A super self-aligned bipolar transistor, comprising:

a semiconductor substrate having a buried collector region;

multiple layers above said collector region;

an emitter window mask above said multiple layers;

a doped collector region wherein the width of the doped collector region are equal to the emitter window mask width;

a horizontal etched region of one of said multiple layers, wherein said horizontally etched region is a polysilicon region and extends a distance greater than a thickness of said polysilicon region;

a base region above said collector region in the horizontally etched area; [and]

an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontally etched region determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region; and

an oxide layer and a Nitride layer above said multiple layers.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Withdrawn)

14. (Canceled)

15. (Original) The apparatus as described in claim 8 wherein the horizontally etched region allows the space between active and inactive base regions to be precisely controlled and also allows the spacing of extrinsic to active emitter and collector regions to be controlled.

16. (Original) The apparatus as described in claim 15 wherein the multiple layers have been etched to the same width as the emitter and collector regions.

17. (Original) The apparatus as described in claim 16 wherein the dimensions of the doped region of the collector is the same as the dimension of the emitter region.

18. (Previously amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing a first oxide layer, a polysilicon layer and a second oxide layer above said collector region;

providing a Nitride emitter window mask above said oxide and polysilicon layers;

providing a wet etching with hydrofluoric acid solutions to etch first and second oxide layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of said polysilicon layer, wherein said horizontal etching is etched a distance greater than a thickness of said polysilicon layer;

providing a base region above said collector region in the horizontally etched area wherein the base region extends horizontally beyond the doped collector region; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said

base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

19. (Original) The method as described in claim 18 further comprising the step of predetermining the length of the horizontally etched region in order to optimize at least one of frequency response or power gain of the super self-aligned bipolar transistor.

20. (Original) The method as described in claim 1 further comprising the step of predetermining the length of the horizontally etched region in order to optimize at least one of frequency response or power gain of the super self-aligned bipolar transistor.

21. (Previously amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein said horizontal etching is performed to a distance greater than a thickness of said polysilicon and whereby said distance may be conformed to provide desired electrical characteristics;

providing a wet etching to remove a final one of said multiple layers;

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

22. (Withdrawn)

23. (Previously amended) The method of claim 21 wherein the desired electrical characteristics are transistor gain and frequency response.